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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/903,705	07/13/2001	Brian Gerard Goodman	TUC920000084US1	9187

7590

11/05/2004

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EXAMINER

WILSON, YOLANDA L

ART UNIT	PAPER NUMBER
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2113

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/903,705

Applicant(s)

GOODMAN ET AL.

Examiner

Yolanda Wilson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-49 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-49 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

SECOND NON-FINAL REJECTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Ogier (US Publication Number 20030095504A1). As per claim 1, Ogier discloses at least a plurality of said processor nodes each having information of relative locations of said processor nodes on said multi-drop bus network on page 15, paragraph 0209-0217. Ogier discloses said plurality of processor nodes each independently testing access to at least one other of said processor nodes on said multi-drop bus network; upon said access testing by any of said plurality of testing processor nodes detecting a failure to access at least one of said other said processor nodes, said failure detecting processor node determining, from said information of relative locations, the processor node having failed access which is closest to said failure detecting processor node; and said failure detecting processor node storing an identification of said closest processor node having failed access on page 16, paragraphs 0226-0232. The multi-drop bus network is defined on page 3, paragraph 0038 with the 'Protocols for establishing link layer links include

Ethernet, PPP...’ As is known in the art Ethernet 10Base-2 and 10Base-5 are bus networks.

3. As per claim 2, Ogier discloses posting an identifier of said closest processor node having failed access at an associated error indicator local to said failure detecting processor node on page 16, paragraphs 0226-0232.

4. As per claim 3, Ogier discloses upon said access testing by any of said plurality of testing processor nodes detecting a failure to access all of said other processor nodes, said failure detecting processor node posting a special identifier at said associated local error indicator on page 16, paragraphs 0226-0232.

5. As per claim 4, Ogier discloses posting an error message representing said identifier to an error log; and subsequently accumulating said posted error messages of said plurality of processor nodes on page 15, paragraphs 0209-0217.

6. As per claim 5, Ogier discloses locking said posted identifier at said error indicator for a predetermined time-out period; and subsequent to expiration of said time-out period, deleting said posted identifier from said associated local error indicator on page 15, paragraphs 0209-0217.

7. As per claim 6, Ogier discloses locking said posted identifier at said error indicator; and responding to an operator initiated signal, deleting said posted identifier from said associated local error indicator on page 15, paragraphs 0209-0217.

8. As per claim 7, Ogier discloses locking said posted identifier at said associated local error indicator; and said displaying processor node retesting said access, and,

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upon absence of an error during a predetermined number of said retests, deleting said posted identifier from said associated local error indicator on page 14, paragraph 0196.

9. As per claim 8, Ogier discloses said multi-drop bus network additionally comprises multiple processor nodes extending from a single drop of said multi-drop bus network, upon said access failure detecting step detecting access failure of a plurality of said multiple processor nodes at said single drop, said step of determining said processor node having failed access additionally comprises determining, from said information of relative locations, said single drop having failed access which is closest to said failure detecting processor node, and selecting one of said multiple processor nodes at said single drop, said failure detecting processor node storing an identification of said selected processor node on page 15, paragraph 0209-0217 and on page 16, paragraphs 0226-0232. The multi-drop bus network is defined on page 3, paragraph 0038 with the 'Protocols for establishing link layer links include Ethernet, PPP...' As is known in the art Ethernet 10Base-2 and 10Base-5 are bus networks.

10. As per claim 9, Ogier discloses one of said multiple processor nodes extending from said single drop of said multi-drop bus network is identified as having a higher priority than other processor nodes extending from said single drop, and wherein said selecting step comprises selecting said multiple processor node having said higher priority on page 14, paragraphs 0195-0196.

11. As per claim 10, Ogier discloses a multi-drop bus network; processor nodes coupled by said multi-drop bus network, each of a plurality of said processor nodes having information providing relative locations of said processor nodes on said multi-

drop bus network on page 15, paragraph 0209-0217. Ogier discloses said plurality of processor nodes each independently testing access to at least one other of said processor nodes on said multi-drop bus network; upon said access testing by any of said plurality of testing processor nodes detecting a failure to access at least one of said other said processor nodes, said failure detecting processor node determining, from said information of relative locations, the processor node having failed access which is closest to said failure detecting processor node, and storing an identification of said closest processor node having failed access on page 16, paragraphs 0226-0232. The multi-drop bus network is defined on page 3, paragraph 0038 with the 'Protocols for establishing link layer links include Ethernet, PPP...' As is known in the art Ethernet 10Base-2 and 10Base-5 are bus networks.

12. As per claim 11, Ogier discloses additionally comprising a local error indicator associated with at least one of said plurality of processor nodes, said failure detecting processor node posting, at said local error indicator associated with said failure detecting processor node, an identifier of said closest processor node having failed access on page 16, paragraphs 0226-0232.

13. As per claim 12, Ogier discloses wherein said plurality of processor nodes, additionally, upon said access testing by any of said plurality of testing processor nodes detecting a failure to access all of said other processor nodes, said failure detecting processor node posting a special identifier at said associated local error indicator on page 16, paragraphs 0226-0232.

14. As per claim 13, Ogier discloses wherein each of said plurality of processor nodes additionally comprises an error log, and, upon detecting said access failure, posts an error message representing said identifier to said error log on page 15, paragraphs 0209-0217.

15. As per claim 14, Ogier discloses wherein at least one of said plurality of processor nodes additionally comprises a timer; and, upon detecting said access failure, locks said posted identifier at said associated local error indicator and starts said timer to time a predetermined time-out period; and responds to expiration of said time-out period of said timer, deleting said posted identifier from said local error indicator on page 15, paragraphs 0209-0217.

16. As per claim 15, Ogier discloses additionally comprising an operator input; and wherein at least one of said plurality of processor nodes, additionally, upon detecting said access failure, locks said posted identifier at said associated local error indicator; and responds to an operator initiated signal at said operator input, deleting said posted identifier from said associated local error indicator on page 14, paragraph 0196.

17. As per claim 16, Ogier discloses wherein at least one of said plurality of processor nodes additionally, upon detecting said access failure, locks said posted identifier at said associated local error indicator; and said displaying processor node retesting said access, and, upon absence of an error during a predetermined number of said retests, deleting said posted identifier from said local error indicator on page 14, paragraph 0196.

18. As per claim 17, Ogier discloses additionally comprising multiple ones of said processor nodes extending from a single drop of said multi-drop bus network; wherein said information of relative locations of said plurality of processor nodes, additionally provides information of said processor nodes at said single drop; wherein each said failure detecting processor node additionally, upon detecting access failure of a plurality of said multiple processor nodes at said single drop, determines from said information of relative locations, said single drop having failed accesses which is closest to said failure detecting processor node, and selects one of said multiple processor nodes at said single drop, said failure detecting processor node storing an identification of said selected processor node on page 15, paragraph 0209-0217 and on page 16, paragraphs 0226-0232. The multi-drop bus network is defined on page 3, paragraph 0038 with the 'Protocols for establishing link layer links include Ethernet, PPP...' As is known in the art Ethernet 10Base-2 and 10Base-5 are bus networks.

19. As per claim 18, Ogier discloses wherein one of said multiple processor nodes extending from said single drop of said multi-drop bus network is identified in said information of relative locations as having a higher priority than other processor nodes extending from said single drop; and wherein each of said plurality of processor nodes additionally, upon detecting said access failure at said single drop, determines from said information of relative locations, said higher priority processor node, and selects and stores an identification of said multiple processor node having said higher priority on page 14, paragraphs 0195-0196.

20. As per claim 19, Ogier discloses wherein said local error indicators comprise character displays of at least one character on page 14, paragraphs 0195-0196.

21. As per claim 20, Ogier discloses said distributed processing system comprising processor nodes coupled by a multi-drop bus network, said processor node comprising: an information table providing relative locations of said processor nodes on said multi-drop bus network; and a processor independently testing access to other said processor nodes on said multi-drop bus network; upon said access testing detecting a failure to access at least one of said other processor nodes, determining, from said information table of relative locations, the processor node having failed access which is closest to said failure detecting processor node, and storing an identification of said closest processor node having failed access on page 15, paragraph 0209-0217 and on page 16, paragraphs 0226-0232. The multi-drop bus network is defined on page 3, paragraph 0038 with the 'Protocols for establishing link layer links include Ethernet, PPP...' As is known in the art Ethernet 10Base-2 and 10Base-5 are bus networks.

22. As per claim 21, Ogier discloses additionally comprising a local error indicator associated with said processor of said failure detecting processor, said processor node posting, at said associated local error indicator, an identifier of said closest processor node having failed access on page 14, paragraphs 0195-0196.

23. As per claim 22, Ogier discloses additionally, upon said access testing detecting a failure to access all of said other processor nodes, said failure detecting processor node posting a special identifier at said associated local error indicator on page 16, paragraphs 0226-0232.

24. As per claim 23, Ogier discloses additionally comprising an error log, and wherein said processor, upon detecting said access failure, posts an error message representing said identifier to said error log on page 15, paragraphs 0209-0217.

25. As per claim 24, Ogier discloses additionally comprising a timer; and wherein said processor, upon detecting said access failure, locks said posted identifier at said associated local error indicator and starts said timer to time a predetermined time-out period; and responds to expiration of said time-out period of said timer, deleting said posted identifier from said associated local error indicator on page 15, paragraphs 0209-0217.

26. As per claim 25, Ogier discloses additionally, upon detecting said access failure, locks said posted identifier at said associated local error indicator; and responds to an operator initiated signal at an operator input, deleting said posted identifier from said associated local error indicator on page 14, paragraph 0196.

27. As per claim 26, Ogier discloses said processor, upon detecting said access failure, locks said posted identifier at said associated local error indicator; and retests said access, and, upon absence of an error during a predetermined number of said retests, deleting said posted identifier from said associated local error indicator on page 14, paragraph 0196.

28. As per claim 27, Ogier discloses wherein said multi-drop bus network comprises multiple processor nodes extending from a single drop of said multi-drop bus network wherein said information table of relative locations of said processor node additionally provides said processor nodes at said single drop on page 15, paragraphs 0209-0217.

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Ogier discloses wherein said processor additionally, upon detecting access failure of a plurality of said multiple processor nodes at said single drop, determines from said information table of relative locations, said single drop having failed access which is closest to said failure detecting processor node, selects one of said multiple processor nodes at said single drop, and stores an identification of said selected processor node on page 16, paragraphs 0226-0232. The multi-drop bus network is defined on page 3, paragraph 0038 with the 'Protocols for establishing link layer links include Ethernet, PPP...' As is known in the art Ethernet 10Base-2 and 10Base-5 are bus networks.

29. As per claim 28, Ogier discloses wherein one of said multiple processor nodes extending from said single drop of said multi-drop bus network is identified in said information table of relative locations as having a higher priority than other processor nodes extending from said single drop; and wherein said processor additionally, upon detecting said access failures at said single drop, determines from said information table of relative locations, said higher priority processor node, and selects and stores an identification of said multiple processor node having said higher priority on page 15, paragraphs 0209-0217.

30. As per claim 29, Ogier discloses wherein said associated local error indicator comprises a character display of at least one character on page 14, paragraphs 0195-0196.

31. As per claim 30, Ogier discloses for isolating failures of a multi-drop bus network in a distributed processing system, said distributed processing system comprising processor nodes coupled by said multi-drop bus network, comprising: computer

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readable program code which causes a computer processor of at least one of a plurality of said processor nodes to store information of relative locations of said processor nodes on said multi-drop bus network on page 15, paragraphs 0209-0217. Ogier discloses computer readable program code which causes said computer processor to test, independently of other of said processor nodes, access to at least one other of said processor nodes on said multi-drop bus network; computer readable program code which causes said computer processor, upon said access testing detecting a failure to access at least one of said other processor nodes, to determine, from said provided information of relative locations, the processor node having failed access which is closest to said failure detecting processor node; and computer readable program code which causes said computer processor to store an identification of said closest processor node having failed access on page 16, paragraphs 0226-0232. The multi-drop bus network is defined on page 3, paragraph 0038 with the 'Protocols for establishing link layer links include Ethernet, PPP...' As is known in the art Ethernet 10Base-2 and 10Base-5 are bus networks.

32. As per claim 31, Ogier discloses additionally comprising computer readable program code which causes said computer processor to post, at a local error indicator associated with said failure detecting processor node, an identifier of said closest processor node having failed access on page 16, paragraphs 0226-0232.

33. As per claim 32, Ogier discloses additionally comprising computer readable program code which causes said computer processor, upon said access testing

detecting a failure to access all of said other processor nodes, to post a special identifier at said associated local error indicator on page 16, paragraphs 0226-0232.

34. As per claim 33, Ogier discloses additionally comprising computer readable program code which causes said computer processor to provide an error log, and which causes said computer processor, upon detecting said access failure, to post an error message representing said identifier to said error log on page 15, paragraphs 0209-0217.

35. As per claim 34, Ogier discloses additionally comprising computer readable program code which causes said computer processor to provide a timer, and which causes said computer processor, upon detecting said access failure, to lock said posted identifier at said associated local error indicator and start said timer to time a predetermined time-out period, and to respond to expiration of said time-out period of said timer, deleting said posted identifier from said associated local error indicator on page 15, paragraphs 0209-0217.

36. As per claim 35, Ogier discloses wherein said computer readable program code additionally causes said computer processor, upon detecting said access failure, to lock said posted identifier at said associated local error indicator, and to respond to an operator initiated signal at an operator input, deleting said posted identifier from said associated local error indicator on page 15, paragraphs 0209-0217

37. As per claim 36, Ogier discloses wherein said computer readable program code additionally causes said computer processor, upon detecting said access failure, to lock said posted identifier at said associated local error indicator, and to retest said access,

and upon absence of an error during a predetermined number of said retests, to delete said posted identifier from said associated local error indicator on page 15, paragraphs 0209-0217.

38. As per claim 37, Ogier discloses wherein said multi-drop bus network comprises multiple processor nodes extending from a single drop of said multi-drop bus network; and wherein said computer readable program code additionally causes said computer processor to provide said information of relative locations of said processor nodes to additionally provide information of said processor nodes at said single drop; and wherein said computer readable program code additionally causes said computer processor, upon detecting access failure of a plurality of said multiple processor nodes at said single drop, to determine from said information of relative locations, said single drop having failed access which is closest to said failure detecting processor node, to select one of said multiple processor nodes at said single drop, and to store an identification of said selected processor node on page 15, paragraph 0209-0217 and on page 16, paragraphs 0226-0232.

39. As per claim 38, Ogier discloses wherein said computer readable program code additionally causes said computer processor to identify, in said provided information of relative locations, one of said multiple processor nodes extending from said single drop of said multi-drop bus network as having a higher priority than other processor nodes extending from said single drop; and wherein said computer readable program code additionally causes said computer processor, upon detecting said access failures at said single drop, to determine from said information of relative locations, said higher

priority processor node, and to select an identification of said multiple processor node having said higher priority on page 15, paragraph 0209-0217 and on page 16, paragraphs 0226-0232.

Claim Rejections - 35 USC § 103

40. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

41. Claims 39-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogier in view of Rockwell (USPN 6204992B1). As appears in claim 39, Ogier discloses a multi-drop bus network; at least one communication processor node for receiving commands, and coupled to said multi-drop bus network to provide a communication link for said commands; each of said processor nodes having information of relative locations of processor nodes on said multi-drop bus network; said processor nodes each independently testing access to other said processor nodes on said multi-drop bus network; upon said access testing by any of said testing processor nodes detecting a failure to access at least one of said other processor nodes, said failure detecting processor node determining, from said information of relative locations, the processor node having failed access which is closest to said failure detecting processor node; and said failure detecting processor node storing an identification of said closest processor node having failed access.

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Ogier fails to explicitly state a robot accessor having a gripper and servo motors for accessing said data storage cartridges, said robot accessor having at least one processor node coupled to said multi-drop bus network for operating said gripper and said servo motors in response to said linked commands.

Rockwell discloses this limitation in column 4, lines 25-35.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a robot accessor having a gripper and servo motors for accessing said data storage cartridges, said robot accessor having at least one processor node coupled to said multi-drop bus network for operating said gripper and said servo motors in response to said linked commands. A person of ordinary skill in the art would have been motivated to have a robot accessor having a gripper and servo motors for accessing said data storage cartridges, said robot accessor having at least one processor node coupled to said multi-drop bus network for operating said gripper and said servo motors in response to said linked commands because a processor can access data stored in the data storage cartridges located in the data storage library. Rockwell discloses this reasoning in column 3, lines 26-36.

42. As per claim 40, Ogier discloses additionally comprising a plurality of local error indicators, each uniquely associated with at least one of said processor nodes, and wherein said failure detecting processor node additionally posts, at said local error indicator associated with said failure detecting processor node, an identification of said closest processor node having failed access on page 16, paragraphs 0226-0232.

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43. As per claim 41, Ogier discloses wherein said processor nodes, additionally, upon said access testing by any of said testing processor nodes detecting a failure to access all of said other processor nodes, said failure detecting processor node posting a special identifier at said associated local error indicator on page 16, paragraphs 0226-0232.

44. As per claim 42, Ogier discloses wherein each of said processor nodes additionally comprises an error log, and, upon detecting said access failure, posts an error message representing said identifier to said error log on page 15, paragraphs 0209-0217.

45. As per claim 43, Ogier discloses wherein at least one of said processor nodes additionally comprises a timer; and, upon detecting said access failure, locks said posted identifier at said associated local error indicator and starts said timer to time a predetermined time-out period; and responds to expiration of said time-out period of said timer, deleting said posted identifier from said associated local error indicator on page 15, paragraphs 0209-0217.

46. As per claim 44, Ogier discloses additionally comprising an operator panel comprising an operator panel processor node and an operator input; and wherein at least one of said processor nodes, additionally, upon detecting said access failure, locks said posted identifier at said associated local error indicator; and responds to an operator initiated signal at said operator input, deleting said posted identifier from said associated local error indicator on page 14, paragraph 0196.

47. As per claim 45, Ogier discloses wherein at least one of said processor nodes additionally, upon detecting said access failure, locks said posted identifier at said associated local error indicator; and said displaying processor node retesting said access, and, upon absence of an error during a predetermined number of said retests, deleting said posted identifier from said associated local error indicator on page 15, paragraphs 0209-0217.

48. As per claim 46, Ogier discloses additionally comprising multiple ones of said processor nodes extending from a single drop of said multi-drop bus network; wherein said provided information of relative locations of said plurality of processor nodes additionally determining said processor nodes at said single drop; wherein each of said processor nodes additionally, upon detecting access failure of a plurality of said multiple processor nodes at said single drop, determines from said information of relative locations, said single drop having failed access which is closest to said failure detecting processor node, and selects one of said multiple processor nodes at said single drop, said failure detecting processor node storing an identification of said selected processor node on page 15, paragraph 0209-0217 and on page 16, paragraphs 0226-0232.

49. As per claim 47, Ogier discloses wherein one of said multiple processor nodes extending from said single drop of said multi-drop bus network is identified in said provided information of relative locations as having a higher priority than other processor nodes extending from said single drop; and wherein each of said plurality of processor nodes additionally, upon detecting said access failures at said single drop, determines from said information of relative locations, said higher priority processor

node, and selects and stores an identification of said multiple processor node having said higher priority on page 15, paragraph 0209-0217 and on page 16, paragraphs 0226-0232.

50. As per claim 48, Ogier discloses wherein said local error indicators comprise character displays of at least one character on page 14, paragraphs 0195-0196.

51. As per claim 49, Ogier fails to explicitly state additionally comprising a plurality of interconnected frames, each having a plurality of said storage shelves, at least one of said frames coupling said at least one robot accessor processor node with said multi-drop bus network, at least one of said frames coupling said at least one communication processor node with said multi-drop bus network, said processor nodes in each of said frame comprising at least one said relative location.

Rockwell discloses this limitation in column 2, lines 57-60 and column 4, lines 25-35. The additional racks disclosed in column 2, lines 57-60 are the additional interconnected frames discloses in claim 49.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a plurality of interconnected frames, each having a plurality of said storage shelves, at least one of said frames coupling said at least one robot accessor processor node with said multi-drop bus network, at least one of said frames coupling said at least one communication processor node with said multi-drop bus network, said processor nodes in each of said frame comprising at least one said relative location. A person of ordinary skill in the art would have been motivated to have a plurality of interconnected frames, each having a plurality of said storage shelves, at

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least one of said frames coupling said at least one robot accessor processor node with said multi-drop bus network, at least one of said frames coupling said at least one communication processor node with said multi-drop bus network, said processor nodes in each of said frame comprising at least one said relative location because more data storage cartridges can be added to the racks to provide more data for storage.


Response to Arguments

52. Applicant's arguments, see pages 17-28 of the amendment, filed 08/03/2004, with respect to the rejection(s) of claim(s) 1-49 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However a new reference has been found and was used in the rejection of claims 1-49 as indicated above. Therefore, Applicant's arguments are now moot in view of the use of the new reference Ogier.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100